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February 4, 2000

Attorney Docket No.: 09464-009001

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: ANDREW J. BURSTEIN AND CHARLES NICKEL

Title: A FLIP-CHIP SWITCHING REGULATOR

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	12
Claims	6
Abstract	1
Declaration (Unsigned)	2
Drawing(s)	8

Enclosures: Unsigned Small Entity Statement
Postcard.

Basic filing fee	$345
Total claims in excess of 20 (25 times $9)	$225
Independent claims in excess of 3 (2 times $39)	$78
Fee for multiple dependent claims	$0
Total filing fee:	$648

Under 37 CFR §1.53(d), no filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE,** to deposit account 06-1050, referencing the attorney document number shown above. A duplicate copy of this transmittal letter is attached.

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ATTORNEY DOCKET NO. 09464-009001

Applicant or Patentee: Andrew J. Burstein, et al.
Serial or Patent No.: Unassigned
Filed or Issued: Herewith
For: A FLIP-CHIP SWITCHING REGULATOR

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(c)) — SMALL BUSINESS CONCERN

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[] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: VOLTERRA SEMICONDUCTOR CORPORATION
Address of Small Business Concern: 42840 Christy Street, Suite 202
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I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled A FLIP-CHIP SWITCHING REGULATOR by inventor(s) ANDREW J. BURSTEIN and CHARLES NICKEL described in:

[X] the specification filed herewith.
[] application serial no. _, filed _.
[] patent no. _, issued _.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent on which this verified statement is directed.

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Attorney's Docket No.: 09464-009001

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: A FLIP-CHIP SWITCHING REGULATOR

APPLICANT: ANDREW J. BURSTEIN AND CHARLES NICKEL

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL444262200US

February 4, 2000

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A FLIP-CHIP SWITCHING REGULATOR

BACKGROUND

The present invention relates generally to voltage regulators, and more particularly to a switching voltage regulator at least partially implemented with flip-chip packaging.

Voltage regulators, such as DC to DC converters, are used to provide stable voltage sources for electronic systems. Efficient DC to DC converters are particularly needed for battery management in low power devices, such as laptop notebooks and cellular phones. Switching voltage regulators (or simply "switching regulators") are known to be an efficient type of DC to DC converter. A switching regulator generates an output voltage by converting an input DC voltage into a high frequency voltage, and filtering the high frequency voltage to generate the output DC voltage. Specifically, the switching regulator includes a switch for alternately coupling and decoupling an input DC voltage source, such as a battery, to a load, such as an integrated circuit. An output filter, typically including an inductor and a capacitor, between the input voltage source and the load filters the output of the switch and thus provides the output DC voltage. The switch is typically controlled by a pulse modulator, such as a pulse width modulator or a pulse frequency modulator, which controls the switch.

Switching regulators are now being fabricated at least partially with integrated circuit techniques. Specifically, some switching regulators are being fabricated in integrated circuit chips with wire bond packaging (in which wires extend from the sides of the chip to the package, and the package has leads that are soldered to a printed circuit board). Unfortunately, one problem with wire bond chips is that they have a large parasitic inductance and resistance.

The parasitic inductance can result in large voltage transients on the integrated circuit. Specifically, although there is an abrupt change in the supply current when switching from the high to low voltage inputs, the current flowing through the parasitic inductor cannot change instantaneously. Thus, some current will continue to flow, causing the voltage on the voltage supply lines to "bounce". If the voltage transients exceed the process limitations of the integrated circuit, there can be damage due to voltage overstress. In addition, if the voltages on the voltage supply lines come too close together or cross, the digital and analog circuitry

in the voltage regulator will fail. Furthermore, large voltage transients create noise which can interfere with the normal operation of analog components of the power regulator. Compensating for this noise requires additional circuitry, at the expense of design time, silicon area and power consumption..

The parasitic resistance of the packaging increases energy dissipation, which wastes energy and creates excess heat. This excess heat can degrade circuit performance, and in order to avoid the degraded circuit performance, it is necessary to use expensive heat sinks or cooling systems, or limit the current flowing through the device.

In view of the foregoing, it would be advantageous to develop a switching regulator with reduced parasitic inductance and resistance.

SUMMARY

In one aspect, the invention is directed to a voltage regulator having an input terminal and an output terminal. The voltage regulator has a printed circuit board, a substrate mounted on the printed circuit board, and a first flip-chip type integrated circuit chip mounted on the substrate. The first integrated circuit chip includes a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal. A filter is disposed to provide a substantially DC voltage at the output terminal, and a control circuit controls the power switch to maintain the DC voltage substantially constant.

Implementations of the invention may include one or more of the following features. The power switch and filter may form a buck-converter topology. The first integrated circuit chip may be mounted on the substrate with an array of solder bumps, and the substrate may be mounted on the printed circuit board with solder balls. The flip-chip type integrated circuit chip may include a p-type region and an n-type region, and the power switch may include a plurality of p+ regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region. Alternating p+ regions may be connected to the input terminal and to an intermediate terminal, and alternating n+ regions may be connected to the intermediate terminal and to ground. At least a portion of the control circuit may be fabricated in a second integrated circuit chip electrically coupled to the printed circuit board separately from the first chip. A portion of the control circuit, such as an interpreter to interpret commands from the portion of the control circuit fabricated on the second chip, or a

sensor that directs measurements to the portion of the control circuit fabricated on the second chip, may be fabricated on the first chip. The filter can be electrically coupled to the printed circuit board or to the substrate separately from the first chip. The first power switch may intermittently couple an intermediate terminal to the input terminal. The first flip-chip type integrated circuit chip may have a second power switch fabricated therein to alternately couple and decouple the intermediate terminal to ground. The filter may be electrically coupled between the output terminal and the intermediate terminal. The first power switch may include a distributed array of PMOS transistors and the second power switch may include a distributed array of NMOS transistors. A rectifier may connect the intermediate terminal to ground. The rectifier may be connected to the printed circuit board separately from the first chip. The filter may include an inductor or a capacitor electrically coupling the first power switch to the output terminal. The inductor is mounted on the substrate or the printed circuit board. The capacitor may be mounted on the substrate. An input capacitor, mounted on the substrate or printed circuit board, may connect the input terminal to ground.

In another aspect, the invention is directed to an integrated circuit chip with a power switch for a voltage regulator fabricated thereon. The chip includes a substrate having a first plurality of doped regions and a second plurality of doped regions and an array of metalized pads fabricated on a surface of the substrate. The first and second pluralities of doped regions are arranged in a first alternating pattern. The array includes a first plurality of pads and a second plurality of pads, with the first and second pluralities of pads arranged in a second alternating pattern. The first plurality of pads are electrically connected to the first plurality of doped regions and to a first terminal of the voltage regulator, and the second plurality of pads are electrically connected to the second plurality of doped regions and to a second terminal in the voltage regulator.

Implementations of the invention may include one or more of the following features. The second alternating pattern may be a first set of alternating stripes, and the first alternating pattern may be a second set of alternating stripes oriented orthogonally to the first set of alternating stripes. The first and second pluralities of doped regions may be p+ regions formed in an n-type well or substrate. The first terminal may be an input terminal and the second terminal may an intermediate terminal. The first and second pluralities of doped regions may be n+ regions formed in a p-type well or substrate. The first terminal may be a

ground terminal and the second terminal is an intermediate terminal. The first plurality of pads may be connected to a first plurality of solder balls and the second plurality of pads may be connected to a second plurality of solder balls interleaved with the first plurality of solder balls across a surface on the chip.

In another aspect, the invention is directed to a power switch for a voltage regulator having an input terminal and an output terminal. The power switch has a PMOS switch fabricated on a chip with a first alternating pattern of source pads and drain pads, an NMOS switch fabricated on the chip with a second alternating pattern of source pads and drain pads, and a substrate having a first signal layer with a first electrode to electrically couple the drain pads of the PMOS and NMOS switches to an intermediate terminal, a second electrode to electrically couple the source pads of the PMOS switch to the input terminal, and a third electrode to electrically couple the source pads of the NMOS switch to ground.

Implementations of the invention may include one or more of the following features. The first and second alternating patterns may be alternating rows. The first electrode may have a body and a first plurality of fingers that extend from the body toward the second electrode, the second electrode may have a body and plurality of fingers that extend toward the first electrode, and the first plurality of fingers may be interdigited with the fingers of the second electrode. The first electrode may have a second plurality of fingers that extend from the body toward the third electrode, the third electrode may have a body and a plurality of fingers that extend toward the first electrode, and the second plurality of fingers may be interdigited with the fingers of the third electrode. Each finger may overlie and be electrically coupled to a row of pads on the chip. The substrate may include a second signal layer formed on an opposite side of the substrate from the first signal layer. Conductive vias through the substrate may electrically connect the first signal layer to the second signal layer. Solder balls may electrically connect the rows of pads to the first, second and third electrodes of the first signal layer.

In another aspect, the invention is directed to a power switch for a voltage regulator. The power switch has a chip having an array of pads formed thereon and a substrate having a signal layer formed thereon. Each pad is connected to a plurality of doped regions to create a distributed array of transistors. The signal layer has a first electrode and a second electrode, the first electrode having a body and a plurality of fingers that extend from the body toward

the second electrode, the second electrode having a body and plurality of fingers that extend toward the first electrode. The fingers of the first electrode are interdigited with the fingers of the second electrode and each finger overlies and is electrically coupled to a row of pads on the chip.

In another aspect, the invention is directed to a voltage regulator having a first flip-chip type integrated circuit chip mounted directly on the printed circuit board. The voltage regulator has an input terminal and an output terminal, and the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal. A filter is disposed to provide a substantially DC voltage at the output terminal, and a control circuit controls the power switch to maintain the DC voltage substantially constant.

Advantages of the invention may include the following. Device reliability, efficiency and temperature control are improved. The power switch package has a low parasitic inductance. Therefore, the package places less stress on the integrated circuit, is less likely to cause the voltages on the inputs to approach too closely, and generates less noise. The power switch package also has a low parasitic resistance, thus reducing excess heat and minimizing the loss of current flowing through the power switch package. Reducing the resistance reduces the amount of power dissipated, thereby making the switching regulator more efficient. The switching regulator can be fabricated in a flip-chip package. The package also permits the circuit density on the chip to be increased, thereby permitting lower cost, smaller area, and more complex chips.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a switching regulator.

Figure 2 is a schematic side view of a flip-chip package from the switching regulator of Figure 1.

Figure 3A is a schematic plan view of a power switch fabricated on a flip-chip according to the invention.

Figure 3B is an enlarged view illustrating the distributed array of parallel transistor used in the power switch of Figure 3A.

Figure 3C is a schematic plan view of a distributed transistor fabricated in a

checkerboard pattern.

Figure 4A is a schematic side view of a pad from the flip-chip of Figure 3A.

Figure 4B is a schematic plan view of the pad of Figure 4A.

Figure 5 is a schematic plan view of the top surface of the substrate nearer to the power switch chip.

Figure 6 is a schematic illustration of the alignment of the flip-chip to the top surface of the substrate.

Figure 7 is a schematic plan view of the bottom surface of the substrate farther from the power switch chip.

Figures 8A-8G are schematic plan views of several configurations for the drain and source pads and the overlying electrodes to enable direct mounting of a flip chip to a printed circuit board.

Figure 9 is a schematic plan view of a switching regulator in which two IC chips are connected separately to a printed circuit board.

Figure 10 is a schematic plan view of a switching regulator in which two IC chips are connected by the same substrate to a printed circuit board.

DETAILED DESCRIPTION

Referring to Figure 1, an implementation of a switching regulator 10 is coupled to a DC input voltage source 12, such as a battery, by an input terminal 20. The switching regulator 10 is also coupled to a load 14, such as an integrated circuit, by an output terminal 24. The switching regulator 10 serves as a DC-to-DC converter between the input terminal 20 and the output terminal 24. The switching regulator 10 includes a switching circuit 16 which serves as a power switch for alternately coupling and decoupling the input terminal 20 to an intermediate terminal 22. The switching circuit 16 includes a rectifier, such as a switch or diode, coupling the intermediate terminal 22 to ground. Specifically, the switching circuit 16 and the output filter 26 may be configured in a buck converter topology with a first transistor 30 having a source connected to the input terminal 20 and a drain connected to the intermediate terminal 22 and a second transistor 32 having a source connected to ground and a drain connected to the intermediate terminal 22. The first transistor 30 may be a P-type MOS (PMOS) device, whereas the second transistor 32 may be an N-type MOS (NMOS)

device. The switching regulator 10 may also include an input capacitor 38 connecting the input terminal 22 to ground.

The switching regulator also includes a controller assembly with a pulse modulator 18 for controlling the operation of the switching circuit 16. The pulse modulator 18 causes the switching circuit 16 to generate an intermediate voltage having a rectangular waveform at the intermediate terminal 22. Although the pulse modulator 18 and the switching circuit 16 are illustrated and described below as a pulse width modulator, the invention is also applicable to various pulse frequency modulation schemes.

The intermediate terminal 22 is coupled to the output terminal 24 by an output filter 26. The output filter 26 converts the rectangular waveform of the intermediate voltage at the intermediate terminal 22 into a substantially DC output voltage at the output terminal 24. Specifically, in a buck-converter topology, the output filter 26 includes an inductor 34 connected between the intermediate terminal 22 and the output terminal 24 and a capacitor 36 connected in parallel with the load 14. During a PMOS conduction period, the voltage source 12 supplies energy to the load 14 and the inductor 34 via the first transistor 30. On the other hand, during an NMOS conduction period, the energy is supplied by the inductor 34. The resulting output voltage V_{out} is a substantially DC voltage. Although the switching circuit 16 and the output filter 26 are illustrated in a buck converter topology, the invention is also applicable to other switching voltage regulator topologies, such as a boost converter or a buck-boost converter topology.

The output voltage is regulated, or maintained at a substantially constant level, by a feedback loop in the controller assembly that includes a feedback circuit 28. The feedback circuit 28 includes circuitry which measures the output voltage and/or the current passing through the output terminal. The measured voltage and current are used to control the pulse modulator 18 so that the output voltage at the output terminal 24 remains substantially constant.

Referring to Figure 2, the switching circuit 16 can be fabricated in a flip-chip package 40 that includes an integrated circuit chip 42 and a substrate 44. The flip-chip package 40 is attached to a printed circuit board (PCB) 46 on which the other components of the power regulator, such as the output filter and feedback circuit, can be mounted. An implementation of the substrate 44 includes a metallized top signal layer 50 which faces the chip 42, a

metallized bottom signal layer 52 on the side of the substrate farther from the chip 42, and vias 54 (shown in phantom) that connect the top signal layer 50 to the bottom signal layer 52. The power switch chip 42 is connected to the top signal layer 50 of the substrate 44 by solder bumps 56 which may be silver, aluminum, copper, brass, an alloy of lead and tin, or another metal or metal alloy. The bottom signal layer 52 of the substrate 44 is connected to the printed circuit board 46 by additional solder balls 58. Of course, the substrate 44 could include three or more signal layers.

As shown in Figure 3A and 3B, each switch in the switching circuit 16 on IC chip 42 is fabricated as a distributed array of parallel transistors. Each switch includes multiple doped regions arranged to form parallel stripes, and alternating stripes are connected to form the source and drain regions of the distributed transistor. Specifically, the NMOS transistor 32 includes alternating stripes of n-doped source regions 60 and drain regions 62 in a p-type well or substrate. The PMOS transistor array 30 will be constructed similarly, with alternating stripes of p-doped source regions and drain regions in an n-type well or substrate. Each pair of source and drain stripes is separated by a gate stripe 64. The IC chip can include two or more metalization layers, e.g., three layers, formed over the semiconductor substrate to carry current from the doped regions to the electrode pads on the surface of the chip.

In another implementation, as shown in Figure 3C, the distributed transistor can be fabricated in a regular array. Specifically, the NMOS transistor 32 includes rectangular n-doped source regions 60' and drain regions 62' laid out in a checkerboard pattern in a p-type well or substrate. The PMOS transistor array 30 will be constructed similarly, with alternating rectangular p-doped source regions and drain regions in an n-type well or substrate. A grid-like gate 64' separates each pair of source and drain regions. Unillustrated metalization layers formed over the semiconductor substrate can carry current from the doped regions to the electrode pads on the surface of the chip.

As shown in Figure 3A, on the surface of the chip, overlying the buried array of distributed transistors, is an array of drain pads and source pads. Specifically, in one implementation, the PMOS switch includes a regular array of source pads 70 and drain pads 72, with alternating rows of the pads connected by the unillustrated metalization layers to the source regions and drain regions, respectively, of the distributed transistor. Similarly, the NMOS switch includes a regular array of source pads 74 and drain pads 76, with alternating

rows of the pads connected by unillustrated metalization layers to the source regions 60 and drain regions 62, respectively. The rows of source and drain pads may be oriented orthogonally to the stripes of source and drain regions in the chip. A possible advantage of this implementation is reduced impedance. Alternatively, the array of distributed transistors can be configured so that the transistors are not direct beneath the drain pads and source pads.

A set of control pads 78 can be located near an edge of the chip 42. The control pads 78 can be connected to gate access lines 66 which are connected to the gate stripes, or the control pads may be connected to unillustrated circuitry on the IC chip 42 which interprets commands generated by the off-chip controller 18 and, in response to the commands, controls the gate access lines. Additional unillustrated circuitry on the IC chip may measure a characteristic of the switching circuit, e.g., the current flowing through the PMOS transistor array 30 and NMOS transistor array 32, and pass the measurement back to the rest of the control circuitry via the control pads 78.

When the flip-chip 42 is connected to the rest of the switching voltage regulator on the printed circuit board 46, the drain pads 70 and 74 will be connected to the intermediate terminal 22, the source pads 72 in the PMOS transistor 30 will be connected to the input terminal 20, and the source pads in the NMOS transistor 32 will be connected to ground. A possible advantage of this distributed array configuration is that current only needs to flow the short distance between adjacent rows of pads, rather than the entire length of the transistor, thereby lowering metal resistance.

Each row of drain or source pads 70, 72, 74, 76 may contain a number of individual pads, e.g., four pads (as shown in Figure 3A) to six pad (as shown in Figure 3B). The center-to-center distance between each pad in a row may be about 300 microns, and the center-to-center distance between each row of pads may be about 250 microns. As shown in Figure 4A, each pad includes a final metal layer 80, such as aluminum, a nitride passivation layer 82, and an under-bump metalization (UBM) layer 84. As shown in Figure 4B, although the pads are illustrated in Figure 3 as square, each pad may be octagonal, or some other shape that is appropriate to maximize circuit performance for a particular application. The UBM layer 84 can have an edge-to-edge distance of about 100 microns, and the final metal layer 80 can having an edge-to-edge distance of about 115 microns.

As previously discussed, the substrate 44 transfers signals from the chip 42 to the

printed circuit board 46. As shown in Figure 5, the top signal layer 50 of the substrate 44 includes an input voltage electrode plane 90, a ground electrode plane 92, and an intermediate voltage electrode plane 94. The intermediate voltage electrode 94 includes a central connecting bar 100, a set of electrode fingers 102 that extend off the central connecting bar 100 toward input voltage electrode 90, and a set of electrode fingers 104 that extend off the central connecting bar 100 toward the ground electrode 92. The input voltage electrode 90 includes a main electrode body 110 and a set of electrode fingers 112 that extend from the main body 110 toward the intermediate voltage electrode 94 and are interdigited with the electrode fingers 102. Similarly, the ground electrode 92 includes a main electrode body 114 and a set of electrode fingers 116 that extend from the main body 114 toward the intermediate voltage electrode 94 and are interdigited with the electrode fingers 104.

Referring to Figure 6, each row of pads on the flip-chip 42 is aligned with one of the electrode fingers in the top signal layer 50. Specifically, each drain pad 70 in the PMOS transistor 30 is aligned with an electrode finger 102 of intermediate voltage electrode 94, and each source pad 72 in the PMOS transistor 30 is aligned with an electrode finger 112 of the input voltage electrode 90. Similarly, each drain pad 74 in the NMOS transistor 32 is aligned with an electrode finger 104 of intermediate voltage electrode 94, and each source pad 76 in the NMOS transistor 32 is aligned with an electrode finger 116 of the ground electrode 92. Small control electrodes 96 are aligned with the control pads 78.

Once assembled, each pad is electrically connected by a solder bump to the appropriate electrode of the top signal layer 50. In general, increasing the number of solder bumps lowers the impedance of the connection between the flip chip and the substrate. The interleaved structure of the electrode fingers on the signal layer 50 and the alternating rows of drain and source pads on the flip-chip 42 provides a very simple configuration that does not require hundreds of individual interconnects. It also provides a very short current path on the chip 42 to each part of the power transistors, thereby reducing on-chip metal resistance and power losses. In addition, the configuration permits the efficient use of field-effect transistors in both the interior and periphery of the chip.

As shown in Figure 7, the bottom signal layer 52 of the substrate 44 includes an intermediate voltage electrode 120, an input voltage electrode 122, and a ground electrode 124. Conductive vias 54 (see Figure 2) connect associated electrodes on the top and bottom

signal layers, so that the bottom intermediate voltage electrode 120 is connected to the top intermediate voltage electrode 94, the bottom input electrode 122 is connected to the top input electrode 90, and the bottom ground electrode 124 is connected to the top ground electrode 92. Additional vias connect the top and bottom control electrodes 96 and 126.

As previously mentioned, solder bumps 58 (shown in phantom in Figure 7) are used to connect the bottom signal layer 52 to the printed circuit board 46. An evenly-spaced array of solder bumps, e.g., a 6x6 array, may be formed on the bottom signal layer 52. Solder bumps 130 connect the input voltage electrode 122 to the input voltage terminal 20, solder bumps 132 connect intermediate voltage electrode 120 to intermediate terminal 22, and solder bumps 134 connect ground electrode 124 to the ground plane of the printed circuit board. In general, increasing the number of solder bumps lowers the impedance of the connection between the substrate and printed circuit board.

In another implementation, the integrated circuit chip 42" may be mounted directly on a printed circuit board. As shown in Figures 8A-8G, the printed circuit board may have an input voltage electrode 90', a ground electrode 92', and an intermediate voltage electrode 94'. The electrodes on the printed circuit board may have different configurations, and the chip 42" may have different numbers and configurations of solder balls to connect the drain and source pads on the chip to the input, ground and intermediate electrodes.

Referring to Figure 9, the other integrated circuit components of the switching regulator 10, such as the feedback circuit 28 and the pulse modulator 18 from the controller assembly, can be fabricated on a second IC chip 140 (which can be a flip-chip or a wire bound chip) that is coupled to the printed circuit board 46 separately from the first IC chip 42. Alternatively, as shown in Figure 10, both the switching circuit IC chip 42 and the second IC chip 140 could be electrically coupled to the printed circuit board 46 by the same substrate 44'. Of course, this will require a different layout of the top and bottom signal layers of the substrate 44' in order to carry signals between the first and second chips 42, 140. As previously noted, the first IC chip 42 can include circuitry that interprets commands generated by the controller assembly, and circuitry that provides feedback to the controller assembly.

The elements of the output filter 26, such as the inductor 3, the filter capacitor 36, and the input capacitor 38 may be mounted at least partly on the substrate 44 (as shown in

phantom in Figure 2). For example, one terminal of the inductor 34 may be connected directly to the intermediate voltage electrode 94. The other terminal of the inductor 34 may be connected to another electrode on the substrate (which would be coupled to the printed circuit board through a via and the bottom signal layer) or directly to the printed circuit board. If the inductor is mounted on the substrate, the filter capacitor 36 may either be mounted on the substrate (as illustrated in Figure 2) or connected directly to the printed circuit board. Alternately, all the elements of the output filter 26, including the inductor 34 and the capacitor 36, may be mounted directly on the printed circuit board 46 (as illustrated in Figure 9). If the switching circuit 16 includes a rectifier instead of a second transistor, the rectifier can be connected to the printed circuit board 46 or to the substrate 44 separately from the first chip 42.

The input capacitor 38 connects the input terminal 22 to ground to compensate for stray inductance on the ground and power supply lines. Placing the input capacitor 38 close to the switching regulator keeps the inductance and resistance low. Preferably, the input capacitor 38 is mounted on the substrate (as illustrated in phantom Figure 2), although it can be connected directly to the printed circuit board (as illustrated in Figure 9).

Numerous modifications to the configuration of the flip-chip design will occur to those of ordinary skill in the art. The intermediate voltage electrode plane 120 need not be a figure-eight shape, and the input and ground electrode planes 122 and 124 need not be rectangular, so long as the vias connect the appropriate portions of the top and bottom signal layers. The solder balls 58 can be larger or smaller than the solder bumps 56, and neither need be disposed in a regular array. The pads can be shapes other than rectangular or octagonal. Other configurations are possible for the distributed array of transistors, and other patterns are possible for the contact pads.

The invention is not limited to the embodiment depicted and described. Rather, the scope of the invention is defined by the appended claims.

What is claimed is:

1. A voltage regulator having an input terminal and an output terminal, comprising:

a printed circuit board;

a substrate mounted on the printed circuit board;

a first flip-chip type integrated circuit chip mounted on the substrate, the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal;

a filter disposed to provide a substantially DC voltage at the output terminal; and

a control circuit to control the power switch to maintain the DC voltage substantially constant.

2. The voltage regulator of claim 1, wherein the power switch and filter form a buck-converter topology.

3. The voltage regulator of claim 1, wherein the integrated circuit chip is mounted on the substrate with an array of solder bumps or solder balls.

4. The voltage regulator of claim 1, wherein the substrate is mounted on the printed circuit board with solder balls.

5. The voltage regulator of claim 1, wherein the flip-chip type integrated circuit chip includes a p-type region and an n-type region, and the power switch includes a plurality of p+ regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region, and wherein alternating p+ regions are connected to the input terminal and to an intermediate terminal, and alternating n+ regions chip are connected to the intermediate terminal and to ground.

6. The voltage regulator of claim 1, wherein a portion of the control circuit is fabricated on the first chip.

7. The voltage regulator of claim 1, wherein the portion of control circuit fabricated on the first chip includes a sensor that directs measurements to the portion of the control circuit

fabricated on the second chip.

8. The voltage regulator of claim 1, wherein at least a portion of the control circuit is fabricated in a second integrated circuit chip electrically coupled to the printed circuit board separately from the first chip.

9. The voltage regulator of claim 8, wherein the portion of control circuit fabricated on the first chip includes an interpreter to interpret commands from the portion of the control circuit fabricated on the second chip.

10. The voltage regulator of claim 1, wherein the filter is electrically coupled to the printed circuit board separately from the first chip.

11. The voltage regulator of claim 1, wherein the filter is electrically coupled to the substrate separately from the first chip.

12. The voltage regulator of claim 1, wherein the first power switch intermittently couples an intermediate terminal to the input terminal.

13. The voltage regulator of claim 12, wherein the first flip-chip type integrated circuit chip has a second power switch fabricated therein to alternately couple and decouple the intermediate terminal to ground.

14. The voltage regulator of claim 13, wherein the filter is electrically coupled between the output terminal and the intermediate terminal.

15. The voltage regulator of claim 13, wherein the first power switch includes a distributed array of PMOS transistors and the second power switch includes a distributed array of NMOS transistors.

16. The voltage regulator of claim 12, further comprising a rectifier connecting the

intermediate terminal to ground.

17. The voltage regulator of claim 16, wherein the rectifier is connected to the printed circuit board separately from the first chip.

18. The voltage regulator of claim 1, wherein the filter includes an inductor electrically coupling the first power switch to the output terminal.

19. The voltage regulator of claim 18, wherein the inductor is mounted on the substrate.

20. The voltage regulator of claim 18, wherein the inductor is mounted on the printed circuit board.

21. The voltage regulator of claim 1, wherein the filter includes a capacitor electrically coupling the output terminal to ground.

22. The voltage regulator of claim 21, wherein the capacitor is mounted on the substrate.

23. The voltage regulator of claim 21, wherein the capacitor is mounted on the printed circuit board.

24. The voltage regulator of claim 1, further comprising an input capacitor connecting the input terminal to ground.

25. The voltage regulator of claim 24, wherein the input capacitor is mounted on the substrate.

26. The voltage regulator of claim 24, wherein the input capacitor is mounted on the printed circuit board.

27. An integrated circuit chip with a power switch for a voltage regulator fabricated

thereon, comprising:

a substrate having a first plurality of doped regions and a second plurality of doped regions, the first and second pluralities of doped regions arranged in a first alternating pattern; and

an array of metalized pads fabricated on a surface of the substrate, the array including a first plurality of pads and a second plurality of pads, with the first and second pluralities of pads arranged in a second alternating pattern;

wherein the first plurality of pads are electrically connected to the first plurality of doped regions and the second plurality of pads are electrically connected to the second plurality of doped regions, and wherein the first plurality of pads are connected to a first terminal of the voltage regulator and the second plurality of pads are connected to a second terminal in the voltage regulator.

28. The chip of claim 27, wherein the second alternating pattern is a first set of alternating stripes.

29. The chip of claim 28, wherein the first alternating pattern is a second set of alternating stripes oriented orthogonally to the first set of alternating stripes.

30. The chip of claim 27, wherein the second alternating pattern is a checkerboard pattern.

31. The chip of claim 27, wherein the first and second pluralities of doped regions are p+ regions formed in an n-type well or substrate.

32. The chip of claim 31, wherein the first terminal is an input terminal and the second terminal is an intermediate terminal.

33. The chip of claim 27, wherein the first and second pluralities of doped regions are n+ regions formed in a p-type well or substrate.

34. The chip of claim 33, wherein the first terminal is a ground terminal and the second

terminal is an intermediate terminal.

35. The chip of claim 27, wherein the first plurality of pads are connected to a first plurality of solder balls and the second plurality of pads are connected to a second plurality of solder balls interleaved with the first plurality of solder balls across a surface on the chip.

36. A power switch for a voltage regulator having an input terminal and an output terminal, comprising:

a PMOS switch fabricated on a chip with a first alternating pattern of source pads and drain pads;

an NMOS switch fabricated on the chip with a second alternating pattern of source pads and drain pads; and

a substrate having a first signal layer with a first electrode to electrically couple the drain pads of the PMOS and NMOS switches to an intermediate terminal, a second electrode to electrically couple the source pads of the PMOS switch to the input terminal, a third electrode to electrically couple the source pads of the NMOS switch to ground.

37. The power switch of claim 36, wherein the first and second alternating patterns are alternating rows.

38. The power switch of claim 36, wherein the first and second alternating patterns are checkerboard patterns.

39. The power switch of claim 36, wherein the first electrode has a body and a first plurality of fingers that extend from the body toward the second electrode, the second electrode has a body and plurality of fingers that extend toward the first electrode, the first plurality of fingers are interdigited with the fingers of the second electrode, and each finger overlies and is electrically coupled to a row of pads on the chip.

40. The power switch of claim 39, wherein the first electrode has a second plurality of fingers that extend from the body toward the third electrode, the third electrode has a body

and a plurality of fingers that extend toward the first electrode, the second plurality of fingers are interdigited with the fingers of the third electrode, and each finger overlies and is electrically coupled to a row of pads on the chip.

41. The power switch of claim 36, wherein the substrate includes a second signal layer formed on an opposite side of the substrate from the first signal layer.

42. The power switch of claim 41, further comprising conductive vias through the substrate to electrically connect the first signal layer to the second signal layer.

43. The power switch of claim 36, further comprising solder balls to electrically connect the rows of pads to the first, second and third electrodes of the first signal layer.

44. A power switch for a voltage regulator, comprising:

a chip having an array of pads formed thereon, each pad connected to a plurality of doped regions to create a distributed array of transistors; and

a substrate having a signal layer formed thereon, the signal layer having a first electrode and a second electrode, the first electrode having a body and a plurality of fingers that extend from the body toward the second electrode, the second electrode having a body and plurality of fingers that extend toward the first electrode, wherein the fingers of the first electrode and are interdigited with the fingers of the second electrode and each finger overlies and is electrically coupled to a row of pads on the chip.

45. A voltage regulator having an input terminal and an output terminal, comprising:

a printed circuit board;

a first flip-chip type integrated circuit chip mounted directly on the printed circuit board, the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal;

a filter disposed to provide a substantially DC voltage at the output terminal; and

a control circuit to control the power switch to maintain the DC voltage substantially constant.

ABSTRACT

A voltage regulator with an input terminal and an output terminal has a printed circuit board, a substrate mounted on the printed circuit board, and a first flip-chip type integrated circuit chip mounted on the substrate. The first integrated circuit chip includes a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal. A filter is disposed to provide a substantially DC voltage at the output terminal, and a control circuit controls the power switch to maintain the DC voltage substantially constant.

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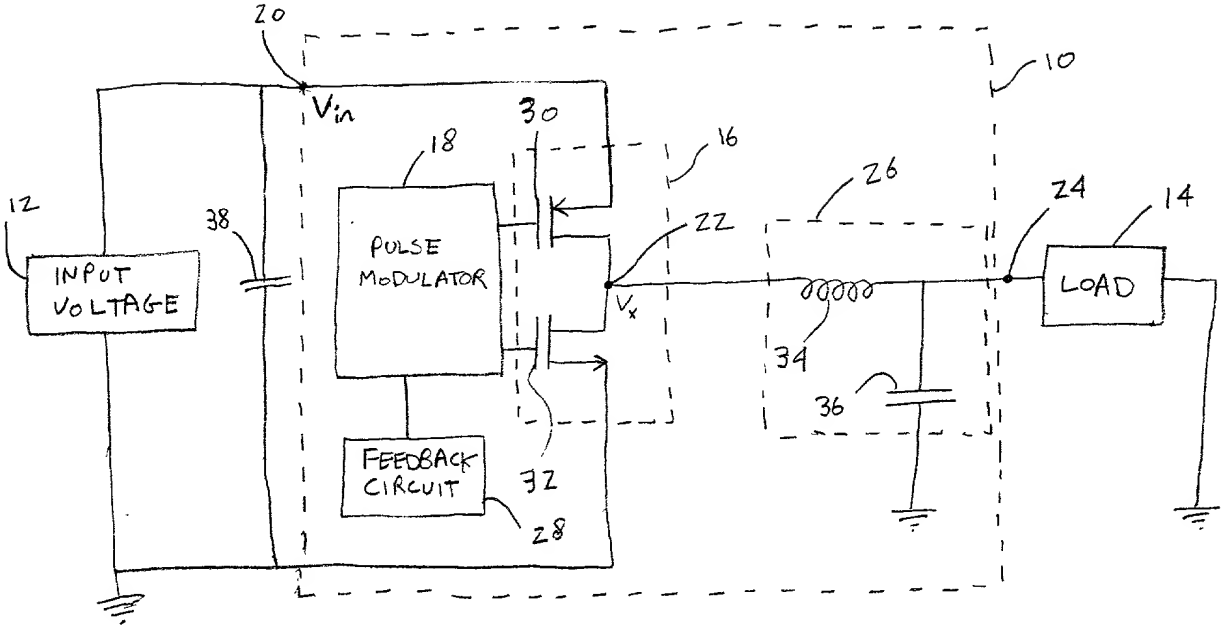
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V_{in}
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PULSE MODULATOR
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LOAD
INPUT VOLTAGE
V_x
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FEEDBACK CIRCUIT
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FIG. 1

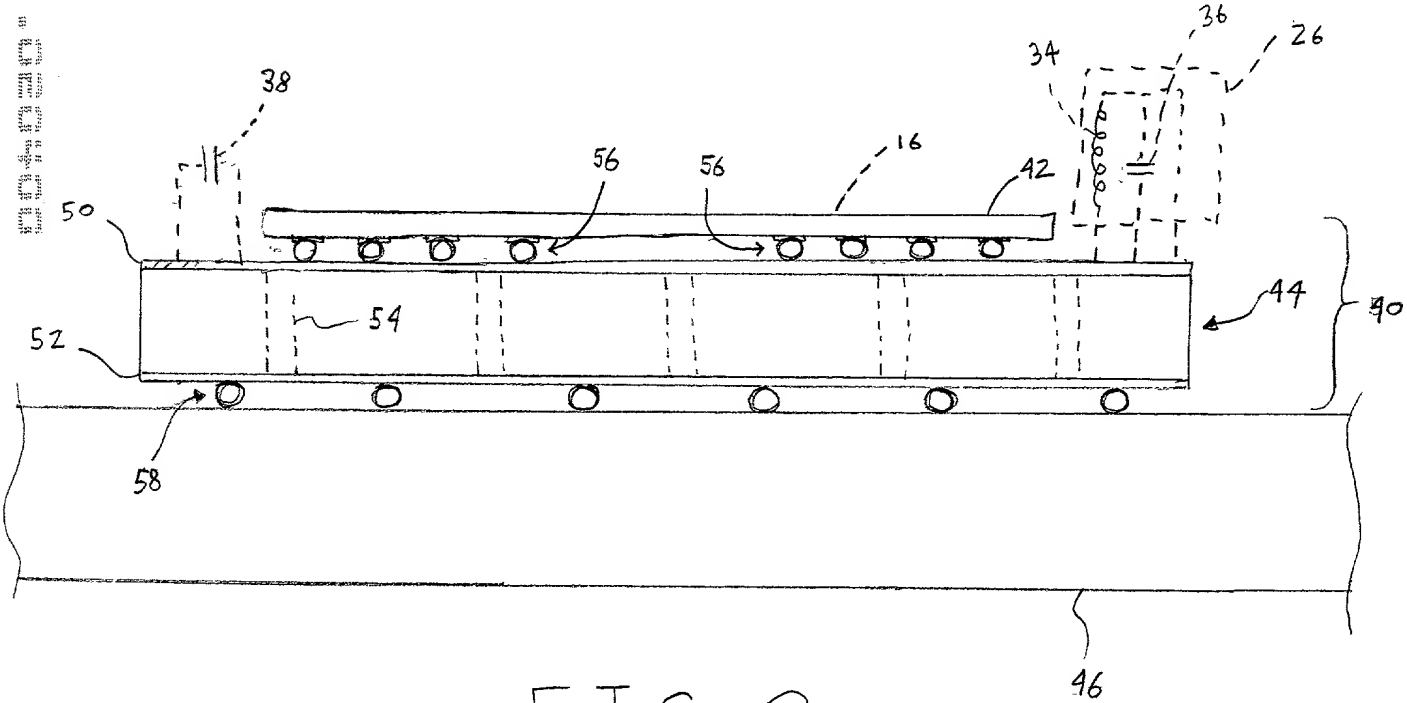
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FIG. 2

FIG. 3A

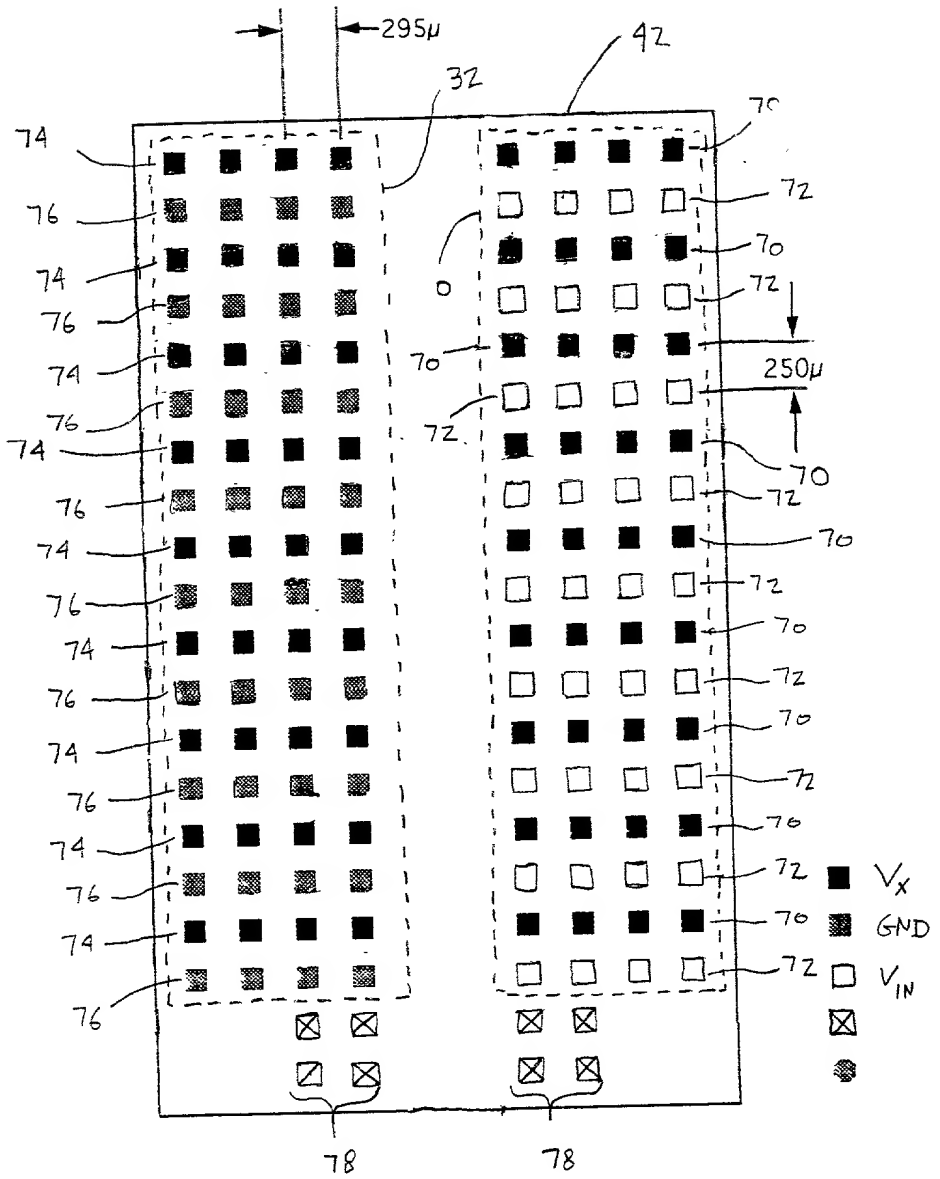
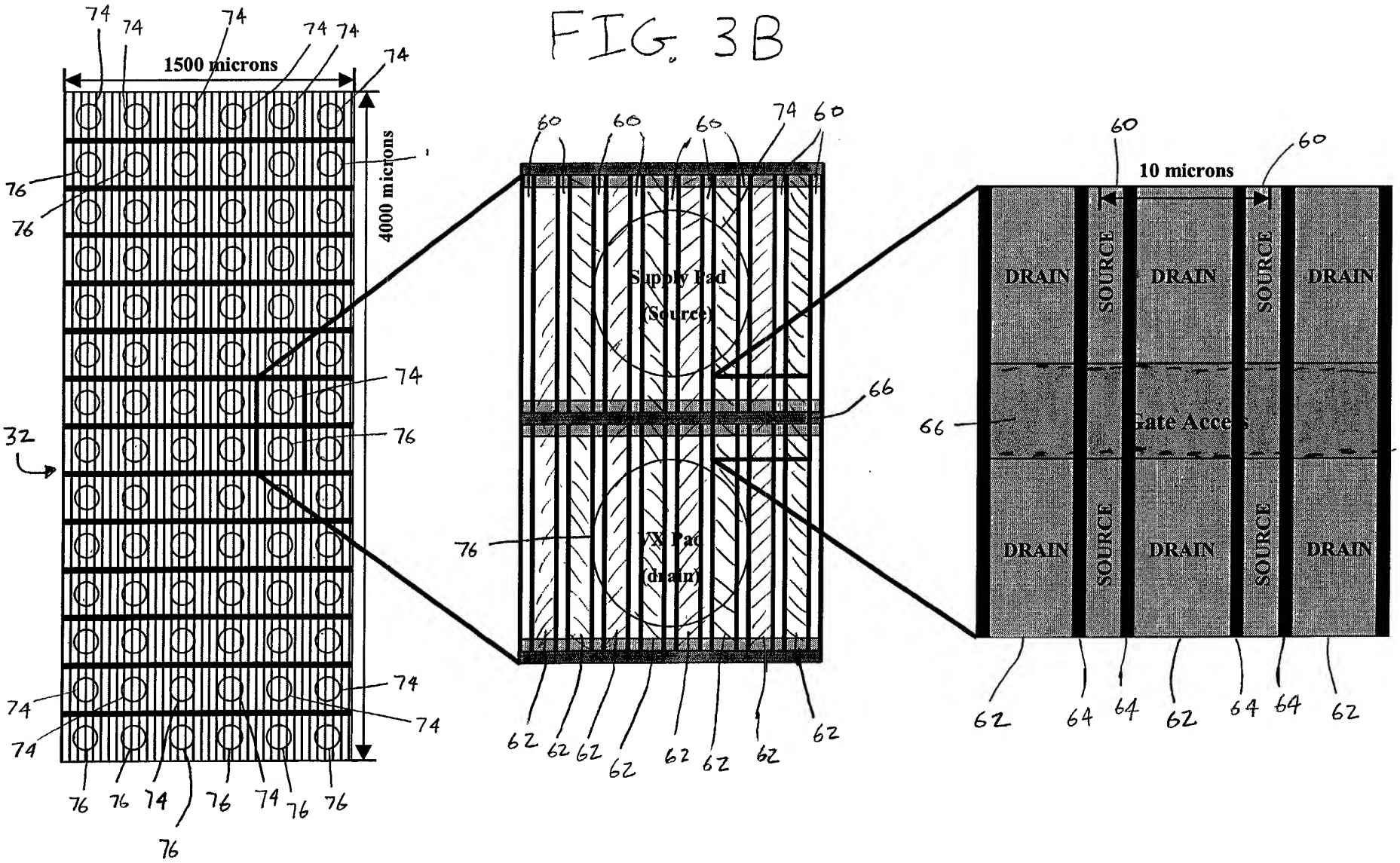


FIG. 3B


1500 microns
4000 microns
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Supply Pad
(Source)
(drain)
Gate Access
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66
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76

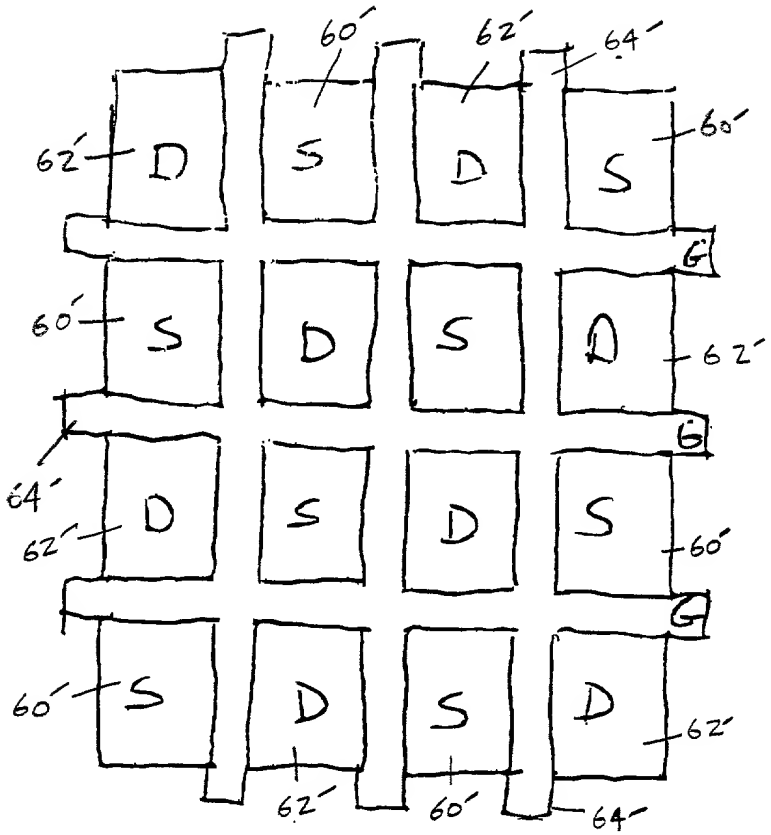


FIG. 3C

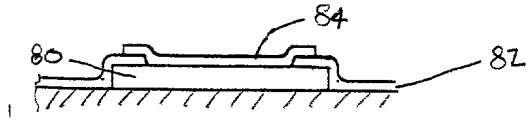


FIG. 4A

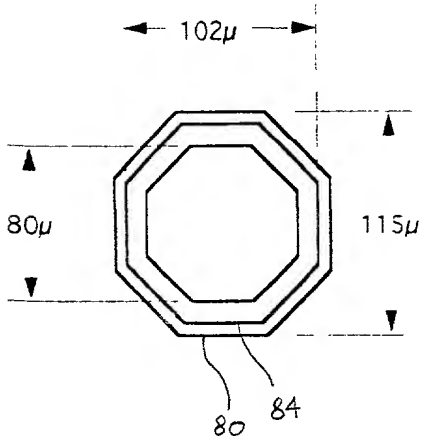


FIG. 4B

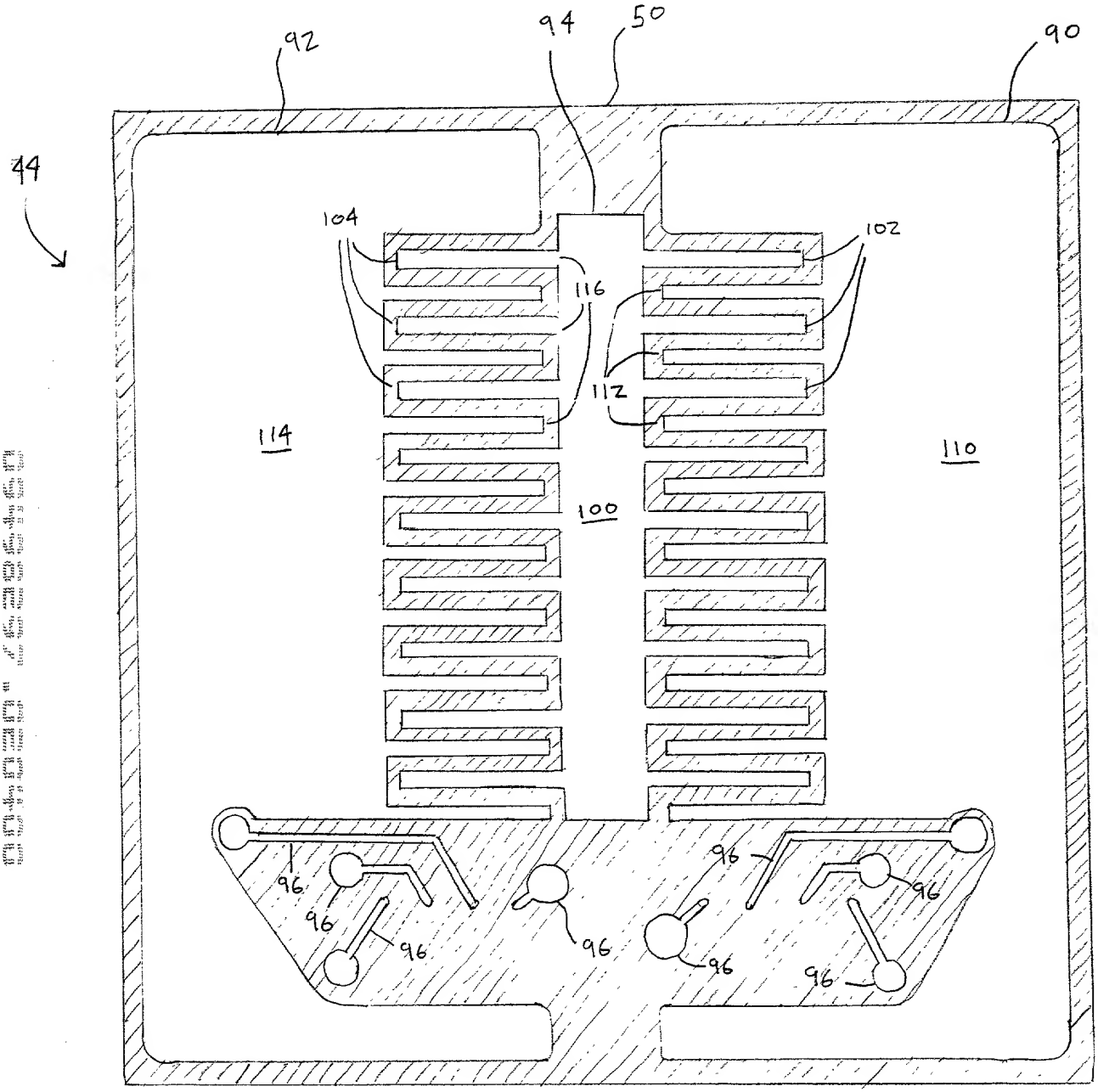
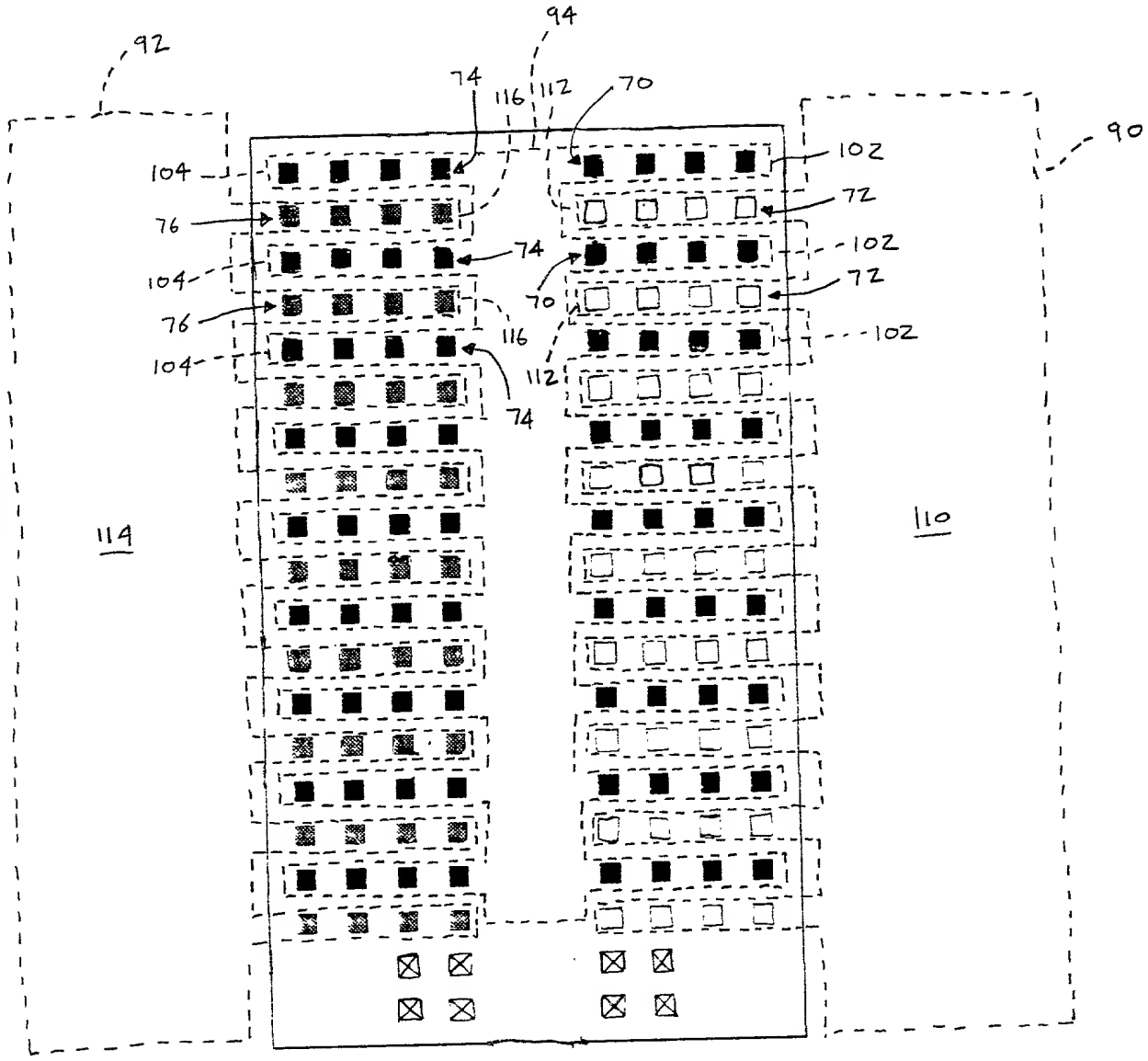


FIG. 5

FIG. 6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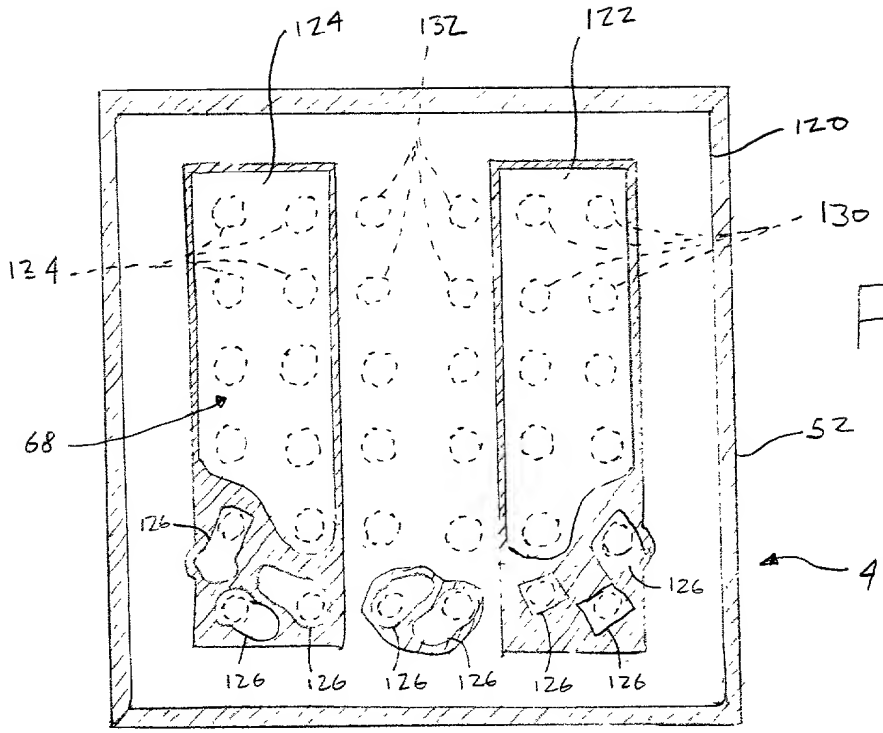


FIG. 7

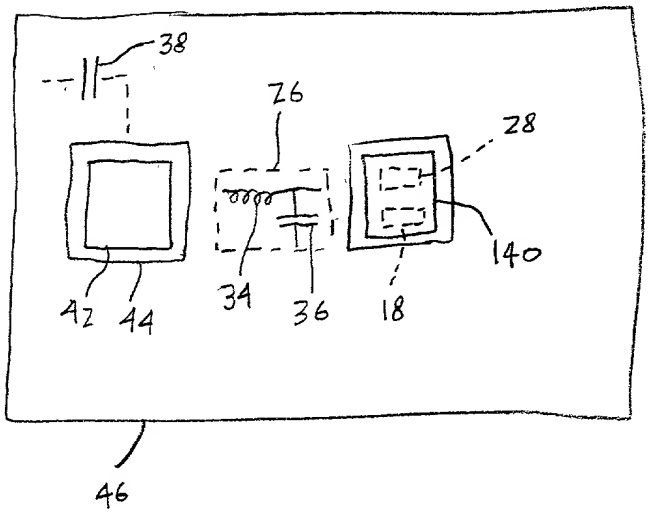


FIG. 9

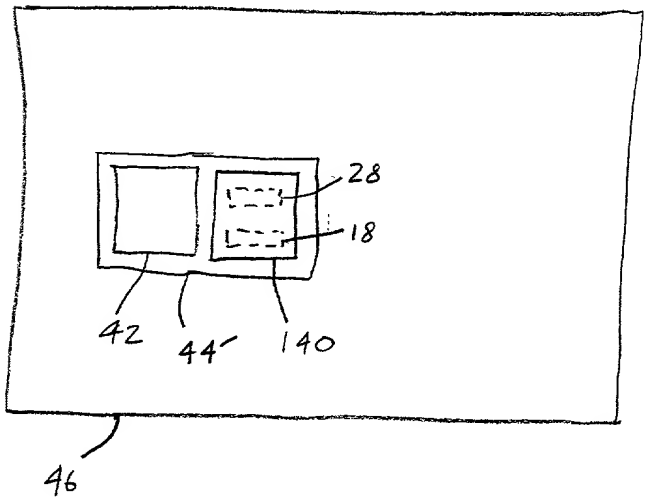
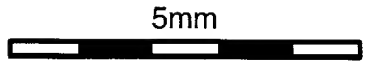


FIG. 10



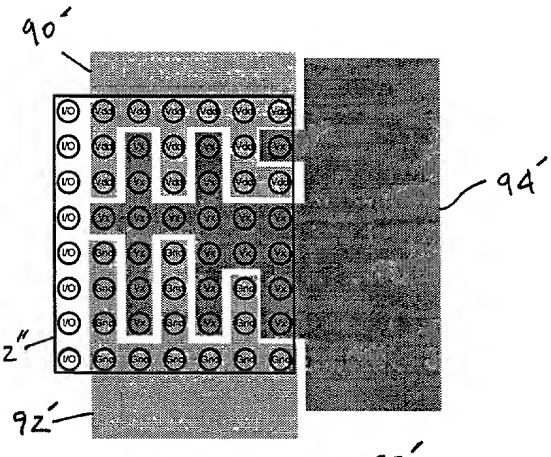


FIG. 8A

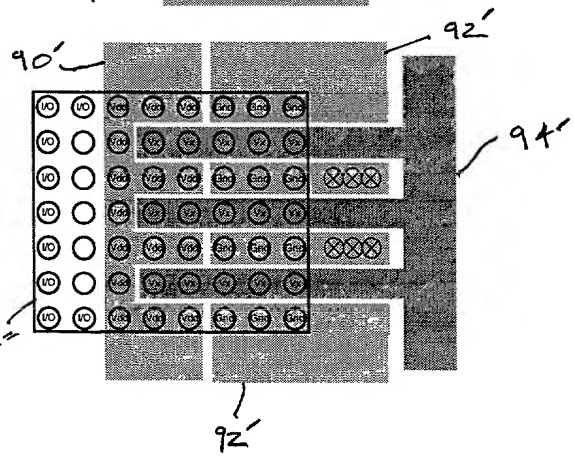


FIG. 8B

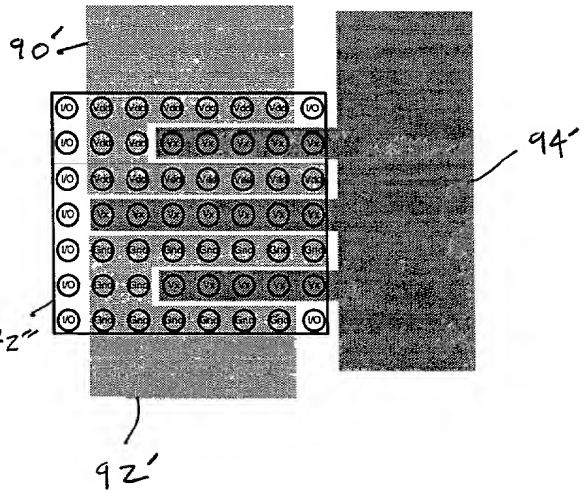


FIG. 8C

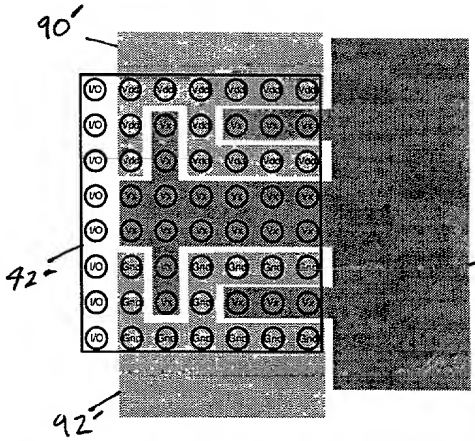


FIG. 8D

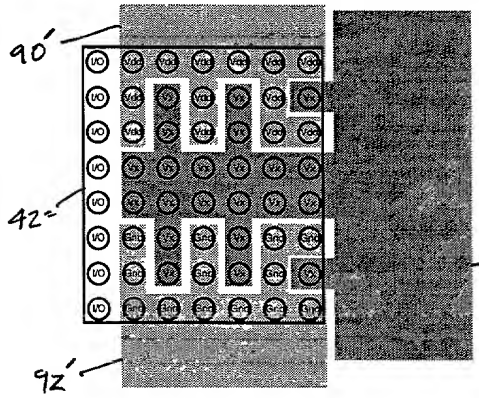


FIG. 8E

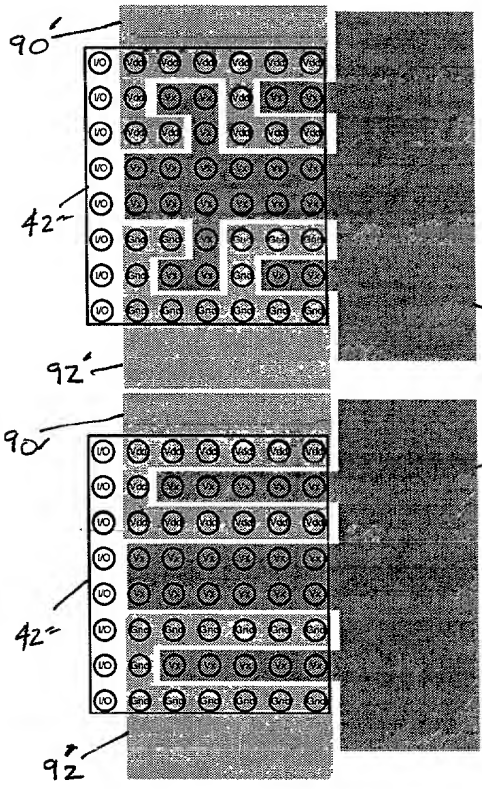


FIG. 8F

FIG. 8G

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A FLIP-CHIP SWITCHING REGULATOR, the specification of which:

[X] is attached hereto.
[] was filed on _ as Application Serial No. _ and was amended on _____.
[] was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Menlo Park, CA 94025

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Inventor's Signature: _____ Date: _____

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